IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph beginning at page 4, line 7, with the following paragraph:

In the display apparatus that uses a PDP, a frame is composed of plural subfields and the subfields to be lit are combined for each cell to represent the gradation scale. FIG.3 shows an example in which a frame is composed of the eight subfields SF1 through SF8. Each subfield comprises the reset period, the address period, and the sustain discharge period, respectively. There can be a case in which a difference appears in the total between the period of the display data supplied from the outside and that of all the subfields, and in such a case, a rest period is provided in the frame. For example, there are two methods for TV display, that is, the Vsync frequency can be 60 Hz or 50 Hz. If the plasma display apparatus is manufactured for 60 Hz and when the apparatus is used at 50 Hz, a ~~reset~~ rest period is provided to adjust the period of a frame. In this ~~reset~~ rest period, no display operation is performed and the length of the rest period is determined in accordance with the display data supplied from the outside. It may be a case where the length remains constant after being determined once, but there can be another case where the total number of pulses, that is, the sum of sustain pulses in all the cells in a frame, is controlled for power control, or another case where the number of the sustain pulses is adjusted in order to keep the brightness ratio among subfields constant regardless of the display load of each subfield, and so on, in other words, when the sustain period (light period) is varied, the length of the rest period is varied according to the display data. As described later, there may be a case where a reset period is not provided to some subfields to improve the display contrast or to abbreviate the reset period.

Please REPLACE the paragraph beginning at page 5, line 34, with the following paragraph:

Generally, it is known that it is a characteristic of human eyes to detect flicker with a frequency lower than 60Hz. In the NTSC method, the Vsync frequency is 60 Hz, but it is 50 Hz in the PAL/SECAM methods employed in Europe, and so on. In a plasma display, images with a high quality are required even in operations with a frequency of 50 Hz. It was found that flicker is not a problem when the arts disclosed in the above-mentioned Japanese Unexamined Patent

Publication (Kokai) No. 3-145691 and Japanese Unexamined Patent Publication (Kokai) No. 7-271325 are applied to the plasma display apparatus using the NTSC method to improve the quality of image, but in the case of the plasma display apparatus using the PAL method, flicker remains a problem even when the above-mentioned arts are applied. These phenomena are described with reference to FIG. 4. In FIGS. 4A, the reset period and the address period are shown as a RESET & ADDRESS PERIOD of a single diagonal line cross-hatch although the portion of a single diagonal line cross-hatch designates the address period in FIG. 3A. This representation of FIG. 4A is used in later figures.

Please REPLACE the paragraph beginning at page 10, line 6, with the following paragraph:

In the method of driving a display apparatus in the second ~~embodiment~~ aspect of the present invention, the rest period is divided into plural rest periods and the divided periods are arranged between plural different subfields. According to the second ~~embodiment~~ aspect of the present invention, when the rest period occurs, it is divided into plural periods and arranged in different positions between subfields, therefore, flicker does not increase if the rest period is provided or the rest period is lengthened because the changes in position of the light emission period of each subfield are small and the increase of the component of a low frequency of the variation of the light emission intensity can be reduced.

Please REPLACE the paragraph beginning at page 10, line 35, with the following paragraph:

In the method of driving a display apparatus in the third ~~embodiment~~ aspect of the present invention in which the brightness of each subfield is determined by the number of applied pulses to be lit in the light period, the brightness of each subfield is determined by the number of pulses to be lit in the light period and the original clock frequency is varied to generate the execute signal at least either in the address period or the light period when the total number of pulses to be lit in a frame is varied.

Please REPLACE the paragraph beginning at page 11, line 8, with the following paragraph:

According to the third ~~embodiment~~ aspect of the present invention, since the original clock frequency is varied, it is possible to vary the number of pulses to be lit without changing the address period and the light period of each subfield and to maintain the relation among the light periods of each subfield constant.

Please REPLACE the paragraph beginning at page 11, line 18, with the following paragraph:

In the method of driving a display apparatus in the fourth ~~embodiment~~ aspect of the present invention, plural arrangement orders of plural subfields in a frame are stored in memory according to the types of still image, animations, and so on, and an arrangement order of subfields selected from among the plural arrangement orders stored according to the determined type of the image is used for display.

Please REPLACE the paragraph beginning at page 11, line 26, with the following paragraph:

As described above, it is impossible to improve every item relating to the image quality with a limited number of subfields. According to the ~~third~~ fourth aspect ~~embodiment~~ of the present invention, images of high quality can be displayed constantly, since the most appropriate arrangement order of subfields is used according to the type of the image.

Please REPLACE the paragraph beginning at page 15, line 34, with the following paragraph:

FIG. 13A is a diagram that shows the frame structure of the method of driving the plasma display apparatus in the fourth embodiment of the present invention, and FIG. 13B is a diagram that shows the variation of the light emission intensity. The plasma display apparatus in the fourth embodiment has almost the same structure as that in the third embodiment, but the control method is different. In the fourth embodiment, a frame is divided into the front frame portion and the rear frame portion, and in the front frame portion, six subfields of 24, 16, 8, 4, 1 and 2 brightness weight are provided in this order, four subfields of 24, 16, 8, and 4 brightness

weight are provided in the rear frame portion in this order, and the rest period is also provided. A next frame wait time is provided between the front frame portion and the rear frame portion. In the fourth embodiment, a signal, the period of which is half the length of the frame, is generated from the Vsync signal and this signal controls the start timings of the front and the rear frames portions. Therefore, the start timings of the front frame portion and the rear frame portion are fixed. When the sustain time of each subfield is varied because of the brightness adjustment, and so on, the "next frame wait time" and the length of the "rest period" in the rear frame portion are adjusted. Therefore, the sustain periods of the two subfields of 24 brightness weight are not changed in position even if the sustain time of each subfield is varied.

Please REPLACE the paragraph beginning at page 16, line 23, with the following paragraph:

FIG.13C shows an example when the rest period is shortened, and in this case the next frame wait time is removed and only the rest period in the ~~real~~ rear frame exists.

Please REPLACE the paragraph beginning at page 16, line 31, with the following paragraph:

FIG.14A is a diagram that shows the frame structure of the method of driving the plasma display apparatus in the fifth embodiment of the present invention, FIG.14B is a diagram that shows the variation of the light emission intensity, and FIG.14C is a diagram that shows the frame structure when there is no rest period. In the frame structure in the fifth embodiment, a total of 10 subfields, that is, subfields of 24, 16, 8, and 4 brightness weight in pairs, respectively, and subfields of 2 and 1 brightness weight each, respectively, are provided and arranged in the order of subfields of 24, 8, 4, 16, 1, 2, 24, 8, 4, and 16 brightness weight. ~~In the former five subfields, the reset period is provided at the front portion, and the reset period is provided at the rear portion in the latter five subfields, and the length of each rest period of the ten subfields is adjusted so that the center position of the sustain period of each subfield is not changed when the length of the rest period of the entire frame is varied.~~ The rest period is divided into ten divided rest periods in correspondence to the subfields. In the former five subfields, the divided rest period is provided at the front portion of the corresponding subfield, and the divided rest period is provided at the rear portion of the corresponding subfield in the latter five subfields, and the length of each rest period is adjusted so that the center position of the sustain period of each

subfield is not changed when the length of the rest period of the entire frame is varied. Therefore, the frame structure is as shown in FIG.14C when the rest period of the entire frame does not exist. In the fifth embodiment, the light emission intensity varies as shown in FIG.14C, and the way the intensity varies is almost constant even if the length of the rest period is varied and only the absolute value of the intensity varies.

Please REPLACE the paragraph beginning at page 18, line 15, with the following paragraph:

In order to realize the driving method in the sixth embodiment, the panel drive control portion 109 in the drive circuit of the PDP apparatus in FIG. 1 is made to have a structure as shown in FIG. 16 so that the period of the sustain pulse can be varied. In the panel drive control portion 109, a CPU121 controls the number of sustain pulses of each subfield according to the brightness adjust signal entered from the outside, the internal power control, and so on. The sustain period of each subfield is constant and the CPU 121 determines the period (frequency) of the sustain pulse based on the number of sustain pulses of each subfield and the length of the sustain period, generates the corresponding control data, and puts out to a D/A converter 122. The D/A converter 122 generates analog signals corresponding to the control data and applies it to a VCO 123. The VCO 123 generates clocks of a frequency corresponding to these analog signals (termed "an original clock frequency"), and supplies them to a scan driver control portion 110 and a common driver control portion 111. In this way, the clock period is varied.